CLAIMS

Please amend the Claims as follows:

1.   (Withdrawn) A system for use by a PU (processing unit) in communicating externally in a symmetrical multiprocessor system, comprising:

PU issue and control logic means;

PU data flow means interconnected to the PU issue and control logic means;

PU channel logic means interconnected to the PU issue and control logic means and the PU data flow means, wherein said PU channel logic means includes:

channel read data means and channel write data means interconnected between the PU data flow means and the PU channel logic means;

channel and data input and output port means interconnected to the PU channel logic means;

channel stall signal output means interconnected from the PU channel logic means to the PU issue command control logic means; and

channel instruction means interconnecting the PU issue and control logic means to the PU channel logic means.

2.   (Withdrawn) The apparatus of claim 1, comprising in addition:

means for keeping track of the number of communications pending with said specified device; and

means for modifying further PU actions when the number of communications with said specified device reaches a given predetermined number.

3.   (Withdrawn) The apparatus of claim 2 wherein the means for modifying PU action operates to prevent further communication with said specified device until the number of communications with said specified device is caused to be altered.

4.   (Withdrawn) The apparatus of claim 1, comprising in addition:

means for assigning a channel for communications with a given external device;

means for placing communications for said given external device in a given storage means;

means for tracking the number of communications, for a given one of read or write instructions, from a PU to a given external device in a given counter associated with said channel that has been assigned;

means for tracking the number of communications, for said given one of read or write instructions, to the PU from the given external device to alter the count in the counter in a direction opposite from the counter movement when said instructions are sent from the PU; and

means for validating data in said given storage means when the count for said channel is at a given value.

5.   (Withdrawn) The apparatus of claim 1, comprising in addition:

means for maintaining a count of register inputs versus outputs; and

means for retrieving data as valid when the count is other than a given predetermined value.

6.   (Withdrawn) The apparatus of claim 1, comprising in addition:

means for maintaining a count of register inputs versus outputs; and

means for preventing further writing of data into said register when the count reaches a given predetermined value.

7. – 13. (Cancelled)

14.   (Withdrawn) A microprocessor, comprising:

read channels;

write channels;

incoming data counting mechanisms for at least some of said read and write channels; and

instruction processing means responding to external device generated instructions requesting a determination of the count in said data counting mechanism of at least one of said write channel and read channels having counting mechanisms.

15. – 18.   (Cancelled)

19.   (Withdrawn) Apparatus for transmitting data between a PU and an external device, comprising:

a data storage register;

means, comprising a part of said register, operable to accumulate data received from multiple writes directed to said register; and

means, comprising a part of said register, operable to transmit all data accumulated in said register in response to a single received read instruction.

20.   (New) A method for tracking communications between a processing unit (PU) and an external device (ED), comprising:

     receiving, by the PU, data from the ED, into a read register;

     sending, by the PU, data to the ED, from a write register;

     incrementing a read channel count upon receipt of inbound data from the ED by the PU;

     issuing a read channel instruction to decrement the read channel count upon processing of received inbound data by the PU;

     incrementing a write channel count upon receipt of outbound data from the PU by the ED;

     issuing a write channel instruction to decrement the write channel count upon transmission by the PU of the outbound data to the ED;

     accessing the read channel count; and

     comparing the accessed read channel count with a predetermined range to determine whether the PU has received data from the ED.

21.   (New) The method as recited in Claim 20, further comprising associating an active channel with the read register and the write register.

22.   (New) The method as recited in Claim 21, wherein issuing a write channel instruction further comprises writing data externally to the PU.

23.   (New) The method as recited in Claim 21, wherein issuing a write channel instruction further comprises writing data to an internal register of the PU.

24. (New) The method as recited in Claim 21, wherein issuing a read channel instruction further comprises returning read data to a PU dataflow.

25. (New) The method as recited in Claim 20, further comprising associating a passive channel with the read register and the write register.

26. (New) The method as recited in Claim 25, wherein issuing a write channel instruction further comprises storing write data locally for an external read operation.

27. (New) The method as recited in Claim 25, wherein issuing a read channel instruction further comprises returning read data to a PU dataflow.

28. (New) A computer program product for tracking communications between a processing unit (PU) and an external device (ED), the computer program product having a computer-readable medium with a computer program embodied thereon, the computer program comprising:

computer code for receiving, by the PU, data from the ED, into a read register;

computer code for sending, by the PU, data to the ED, from a write register;

computer code for incrementing a read channel count upon receipt of inbound data from the ED by the PU;

computer code for issuing a read channel instruction to decrement the read channel count upon processing of received inbound data by the PU;

computer code for incrementing a write channel count upon receipt of outbound data from the PU by the ED;

computer code for issuing a write channel instruction to decrement the write channel count upon transmission by the PU of the outbound data to the ED; and

computer code for accessing the read channel count; and

computer code for comparing the accessed read channel count with a predetermined range to determine whether the PU has received data from the ED.

29.   (New) The computer program product as recited in Claim 28, further comprising computer code for associating an active channel with the read register and the write register.

30.   (New) The computer program product as recited in Claim 29, wherein issuing a write channel instruction further comprises writing data externally to the PU.

31.   (New) The computer program product as recited in Claim 29, wherein issuing a write channel instruction further comprises writing data to an internal register of the PU.

32.   (New) The computer program product as recited in Claim 29, wherein issuing a read channel instruction further comprises returning read data to a PU dataflow.

33.   (New) The computer program product as recited in Claim 28, further comprising computer code for associating a passive channel with the read register and the write register.

34.   (New) The computer program product as recited in Claim 33, wherein issuing a write channel instruction further comprises storing write data locally for an external read operation.

35.   (New) The method as recited in Claim 33, wherein issuing a read channel instruction further

comprises returning read data to a PU dataflow.